29.1 A 2W CMOS Hybrid Switching Amplitude Modulator for EDGE Polar Transmitters

Tae-Woo Kwak[1], Min-Chul Lee[1], Bae-Kun Choi[2], Hanh-Phuc Le[1], Gyu-Hyeong Cho[1]

[1]KAIST, Daejeon, Korea
[2]Magnachip Semiconductor, Cheongju, Korea

Polar transmitters are known as good candidates for high data-rate systems using amplitude variations like EDGE, WCDMA, and WLAN because they can obtain high efficiency by using efficient switched-mode RF PAs. In particular, recent efforts have reduced power consumption by replacing LDO linear modulators in the amplitude path with switching modulators. Nevertheless, LDO modulators are still used in most polar transmitters because of the limited bandwidths of switching modulators. Essentially, in the course of splitting a complex signal into its amplitude and phase components, the BW of each component becomes wider than that of the original signal [1]. Moreover, it is difficult for a switching modulator to follow a high-frequency magnitude signal efficiently since high switching frequencies are required and switching loss increases with switching frequency. Therefore, switching modulators have either been used in envelope tracking transmitters, which require less BW than polar transmitters, or have been implemented with external components or expensive high-speed processes such as GaAs or SiGe. A CMOS amplitude modulator based on the concept of interleaving delta modulation was suggested for polar transmitters in [2]. However, it consumes a lot of power and requires many external components. In this paper, the amplitude modulator shown in Fig. 29.1.1 is designed to meet Class-E2 EDGE requirements regarding output power and spectral mask margin. If an RF PA output power is 26dBm with a maximum efficiency of 40%, it is equivalent to about a 9Ω load. Therefore, this amplitude modulator is designed to drive a PA with an equivalent impedance of 4Ω while its output voltage varies from 0.4 to 3V at V_{dd} = 3.5V.

The modulator presented here has a hybrid structure consisting of a wideband linear amplifier as a voltage source and a switching amplifier as a CCCS to obtain both high speed and high efficiency. The former primarily controls the output voltage (v_o) with good linearity and the latter efficiently supplies most of the output current (i_o) by sensing and amplifying the output current (i_a) of the former. Although this concept has been suggested for audio and envelope-tracking applications [3], it has not been used for a polar transmitter in a CMOS process because it was too difficult to design a linear amplifier with a wide BW, a low output impedance (Z_{out}) and a high current driving capability.

We suggest two methods to mitigate the design difficulty in the linear amplifier. One method is to make the current loop-gain β higher and wider BW, which helps reduce i_a because the output current is $i_o = i_a + i_d = (1 + \beta) \cdot i_a$ as shown in Fig. 29.1.2. In this design, therefore, PWM control with a 2MHz switching frequency (f_s) is used instead of hysteretic control. While the f_s of hysteretic control varies according to v_o, the f_s of PWM control is constant, which makes the unity-gain frequency (f_T) constant as well. The switching stage has a wide f_T of 460kHz. One zero is inserted into the integrator for loop compensation because there are two poles resulting from the integrator and the inductor in the current loop. The other method is to add a feedforward path. The linear amplifier must provide signal current in addition to ripple current (i_{rip}) to prevent v_o from being distorted by the phase lag of the switching stage in the high-frequency region. The feedforward path removes this burden from the linear amplifier if it has lead compensation so that it can cancel the delay of the integrator and the inductor.

The BW of linear amplifier should be higher than 2MHz because that of the switching amplifier is too narrow to meet the EDGE spectral requirement [1]. A low Z_{out} at the switching frequency and its harmonics is also an essential characteristic to prevent the output ripple voltage (v_{rip}) from violating the spectral requirement of -60dB. Since v_{rip} must be less than about 20mV$_{pp}$ given the value of v_o, the Z_{out} of the linear amplifier should be less than about 200mΩ at 2MHz if an i_{rip} of nearly 100mA$_{pp}$ is generated by the 4μH inductor.

Several CMOS output stages have used common-source (CS) or source-follower (SF) configurations. However, a CS output stage [4] has inherently high Z_{out}, and a SF output stage has a limited output swing unsuitable for rail-to-rail operation. Neither the CS output stage with local feedback using an OTA [5] nor the composite output stage composed of CS and SF stages [6] can implement the desired Z_{out} because of the limited loop gain at high frequency. Thus, the new class-AB output buffer shown in Fig. 29.1.3 is used. SF transistors (M_{NSF} and M_{PSF}) as voltage sources and CS transistors (M_{PCS} and M_{NCS}) as CCCS's constitute four local loops in the middle range of v_o, respectively. During positive output swings, M_{NSF} is turned off by M_{PR}, and two loops (M_{PSF}-M_{PCS}, M_{PSF}-M_{NCS}) sink or source i_{rip} to eliminate v_{rip}. During negative output swings, M_{PSF} is turned off by M_{NR}, and two loops (M_{NSF}-M_{PCS}, M_{NSF}-M_{NCS}) perform the same function. Each loop operates in the manner of the current loop shown in Fig. 29.1.2. By turning off M_{PR} or M_{NR} near each supply rail just before the output is clipped, rail-to-rail control is possible. A Class-AB bias control circuit is added to reduce the distortion of the output transistors by guaranteeing that a certain minimum current flows. By inserting a selected minimum output current into the cascode transistors, the bias control becomes faster than the method suggested in [4]. Compensation capacitors and resistors are determined to stabilize each local loop under any load condition. If the slowest loop composed of M_{PSF} and M_{PCS} is stable, the other loops are also stable. The linear amplifier has an f_T of about 10MHz, a Z_{out} of about 0.2Ω and a current driving capability of approximately 300mA.

Although the linear amplifier has a low Z_{out}, i_{rip} should be reduced to reduce both v_{rip} and power consumption. Thus, a single inductor is replaced by a 3rd-order filter with L_1 larger than L_2 as shown in Fig. 29.1.4. Current loop remains stable because the damping resistor R_d and a zero from the integrator cancel two poles, and the remaining pole exists outside f_s. In addition, by adding current feedback through R_{cf}, R_d can be further reduced to decrease i_{rip} without a loss of stability.

Waveforms for a 50kHz square-wave signal with a 4Ω load are shown in Fig. 29.1.5. Input and output voltage waveforms for a 160kHz full-wave rectified signal with an 8Ω load are also presented in Fig. 29.1.6. Because the rectified input signal is generated on the PCB, it has some distortion near the zero crossing points. The hybrid switching modulator can supply a maximum 2.25W to a 4Ω load with 88.3% efficiency. The linear amplifier typically dissipates nearly 30mW and the maximum v_{rip} is 12mV$_{pp}$. This chip is fabricated using a 0.35μm CMOS process with an area of 4.7mm^2. Figure 29.1.7 shows a micrograph of the chip.

Acknowledgement:
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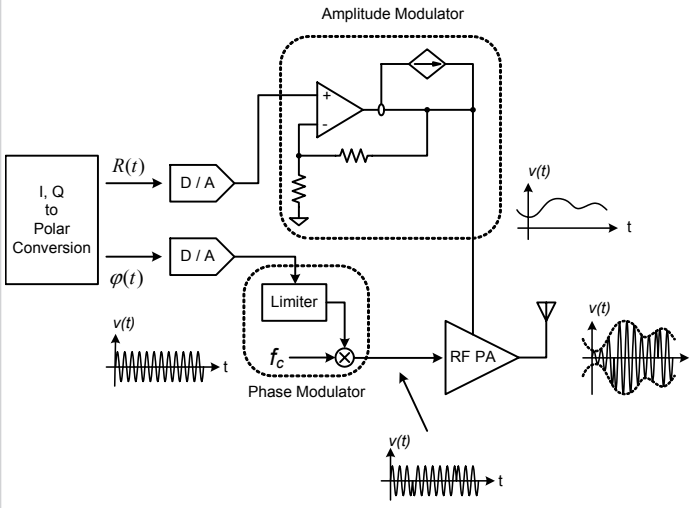

Figure 29.1.1: Block diagram of polar transmitter.

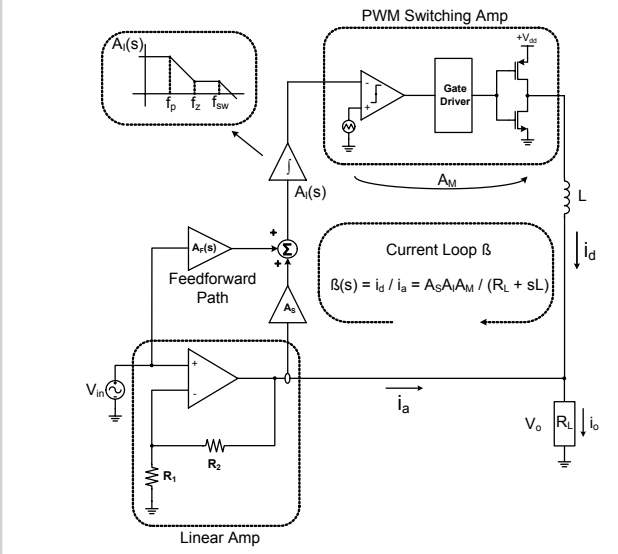

Figure 29.1.2: Simplified block diagram of hybrid switching amplitude modulator.

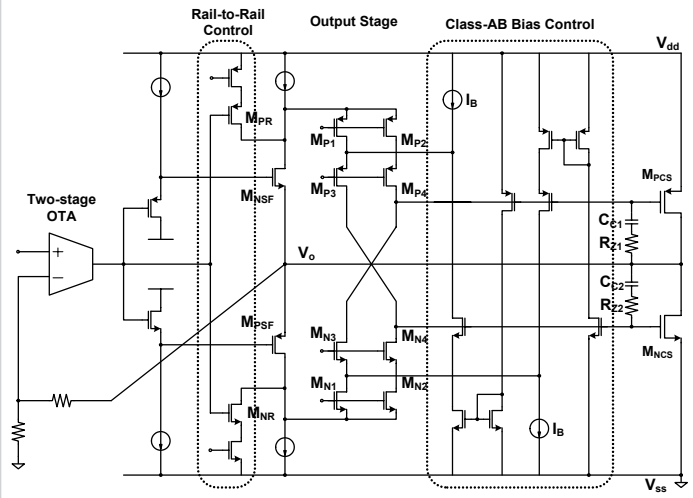

Figure 29.1.3: Linear amplifier with class-AB low output-impedance buffer.

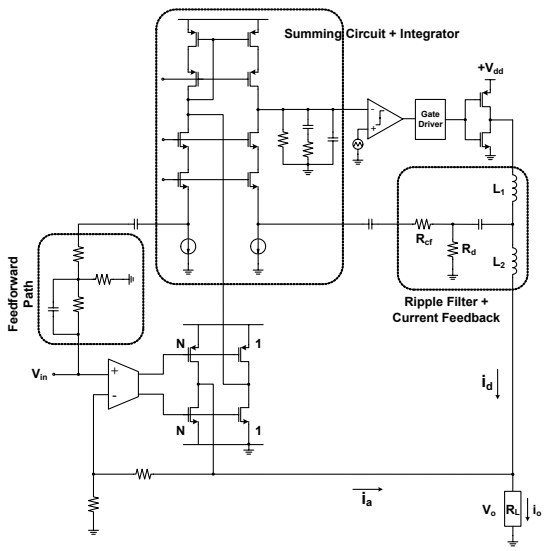

Figure 29.1.4: Detailed block diagram of hybrid switching amplitude modulator.

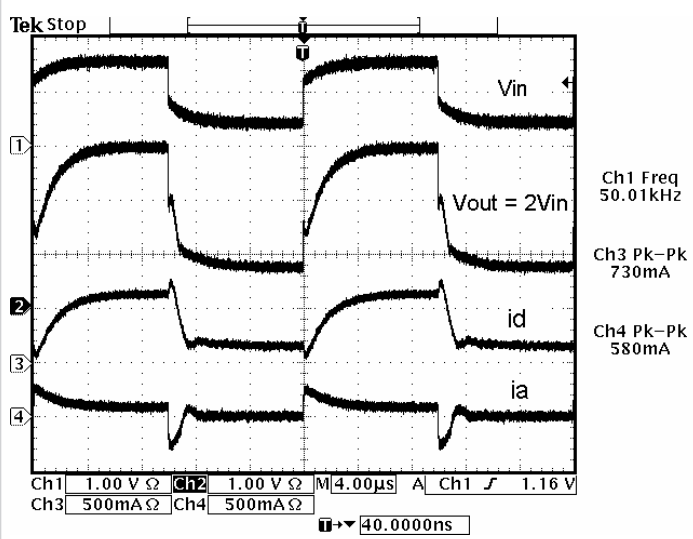

Figure 29.1.5: Measured waveforms for a 50kHz square-wave signal with a 4Ω load.

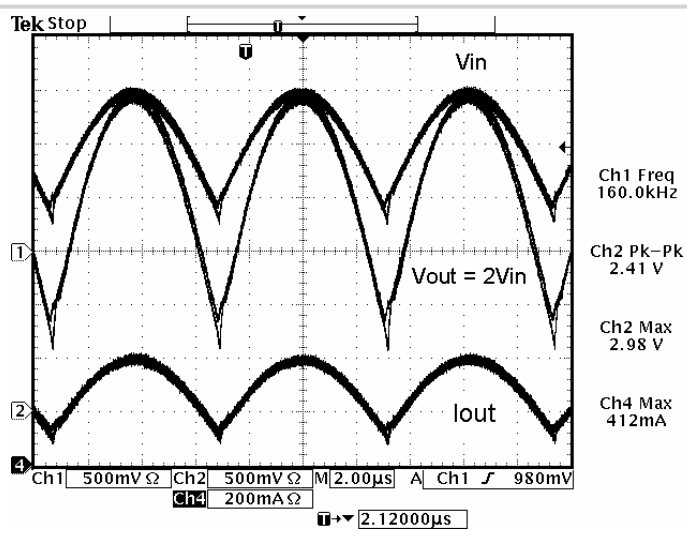

Figure 29.1.6: Measured waveforms for a 160kHz full-wave rectified signal with an 8Ω load.

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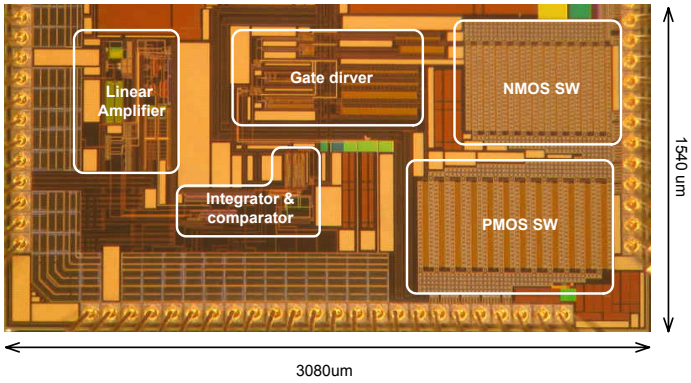

Figure 29.1.7: Chip micrograph.

